REMARKS

This communication is in response to the Office Action dated July 19, 2004. Claims 1-21 are pending in the present Application. Claims 1, 2 and 11-21 are rejected. Claims 3-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-21 remain pending in the present Application.

The present invention is a streamlined efficient cache coherency protocol system and method for a multiple processor one chip (MPOC) system. In one embodiment, a cache coherency maintenance system embedded on a single substrate is disclosed. The system includes a plurality of cache memories, a plurality of processor cores and a coherency maintenance system bus. The cache memories include a memory unit (e.g. a cache line) for storing information that is utilized by the processor cores. At least one of the processor cores is coupled to and associated with one of the cache memories. The system bus communicates the information between the cache memories and the processor cores in accordance with a coherency protocol.

Moreover, the invention is a system that facilitates linking of such related information in a manner that a system user may quickly and easily gain access to particular items of business information, and vice versa. The invention is particularly applicable in the field of compliance by business entities with government product standards.

§103 Rejections

Claim 11

For ease of review, Applicant reproduces independent claim 11 herein below:

11. A coherency maintenance system comprising:

a plurality of cache memories including a cache line for storing information;

a plurality of processor cores included on a single substrate for processing instructions and information stored in said plurality of cache memories wherein one of said plurality of processor cores is coupled to and associated with one of said plurality of cache memories; and

a coherency system bus for providing coherency in accordance with a memory coherency maintenance method, wherein said memory coherency maintenance method maintains coherency throughout a shared memory model including said plurality of cache memories.

The Examiner states:

> **Claim 11 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Carpenter et al. (Carpenter) US Patent 6,115,804 in view of Cherabuddi US Patent Application Pub No. 2002/018445.**

Applicant respectfully disagrees with the Examiner's rejection. In the embodiment of claim 11, a cache coherency maintenance system embedded on a single substrate is recited. The system includes a plurality of cache memories, a plurality of processor cores and a coherency maintenance system bus. The cache memories include a memory unit (e.g. a cache line) for storing information that is utilized by the processor cores. At least one of the processor cores is coupled to and associated with one of the cache memories. The system bus communicates the information between the cache memories and the processor cores in accordance with a coherency protocol.

Carpenter discloses a non-uniform memory access (NUMA) computer system that includes first and second processing nodes that are each coupled to a node interconnect. The first processing node includes a system memory and first and second processors that each have a respective one of first and second cache hierarchies, which are coupled for communication by a local interconnect. The second processing node includes at least a system memory and a third processor having a third cache hierarchy. The first cache hierarchy and the third cache hierarchy are permitted to concurrently store an unmodified copy of a particular cache line in a recent coherency state from which the copy of the particular cache line can be sourced by shared intervention. In response to a request for the particular cache line by the second cache hierarchy, the first cache hierarchy sources a copy of the particular cache line to the second cache hierarchy by shared intervention utilizing communication on only the local interconnect and without communication on the node interconnect

Applicant asserts that Carpenter does not disclose a plurality of processor cores ***on a single substrate*** as recited in claim 11 of the present invention. Carpenter relates to a non-uniform memory access computer system that includes first and second processing nodes that are each coupled to a node interconnect. Although Carpenter discloses the implementation of a plurality of processor cores **12**, these processor cores **12** are in a computer system **6** not on a single substrate as recited in claim 11 of the present invention.

The Examiner asserts that Cherabuddi discloses a plurality of processor cores on a single substrate for the purpose of providing capability of parallel processing and decreasing the size and power consumption and increasing the speed by decreasing the

distance among the components. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a plurality of processor cores included on a single substrate as shown in Cherabuddi into the teaching of Carpenter thereby resulting in the invention as claimed. Applicant disagrees with the Examiner's assessment.

When making an obvious rejection under 35 U.S.C. § 103, a necessary condition is that the combination of the cited references must teach or suggest all claim limitations. If the cited references do not teach or suggest every element of the claimed invention, then the cited references fail to render obvious the claimed invention, i.e. the claimed invention is distinguishable over the combination of the cited references.

Applicant further asserts that obviousness must be determined in the context of what the prior art teaches. For reference structures to be properly combined and thereby render a claimed invention obvious, there must be some motivation for the combination i.e. there must be some teaching, suggestion, or incentive to make the combination claimed by the applicant. *Northern Telecom, Inc. v. Datapoint Corp.* 15 USPQ2d 1321, 1323 (CAFC 1990). ***Motivation coming from the applicant's own disclosure is not sufficient.*** Nor is it sufficient that those of ordinary skill in the art had the capability to combine the referenced structure or understood the advantages of the combination. Although an Examiner may suggest that the structure of a primary prior art reference *could* be modified in view of a secondary prior art reference to form the claimed structure, the mere fact that the prior art *could* be so modified does not make the modification obvious ***unless the prior art suggested the desirability of the modification.*** *In re Newell,* 891 F.2d 899, 13 USPQ2d 1248 (CAFC 1989). (Emphasis added.)

Applicant asserts that the Examiner has provided no motivation, other the Applicant's own specification, to combine the cited references. This is the essence of hindsight reasoning and provides an insufficient basis to reject a claim.

Furthermore, to reinstate an argument from the response filed on 4/22/04, Carpenter does not disclose the employment of ***a coherency system bus*** as recited in claim 11 of the present invention. Carpenter discloses the implementation of node controllers that recognize M, S, and I states and consider the E state to be merged into the S state. That is the node controllers assume that data held exclusively by a remote cache has been modified, whether or not the data has actually been modified, and do not distinguish between the S and R states for remotely held data. (See Carpenter col. 5 lines 3-11). Applicant accordingly asserts that a coherency system bus a recited in claim 11, is different from the disclosed node controller of the Carpenter reference.

Consequently, Applicant asserts that the present invention as recited in the independent claim 11 is patentable over the Examiner's proposed rejection based on a two-fold argument. First, the Examiner has provided no motivation, other the Applicant's own specification, to combine the cited references. This is the essence of hindsight reasoning and provides an insufficient basis to reject a claim. Lastly, Carpenter does not disclose the employment of ***a coherency system bus*** as recited in claim 11 of the present invention. Claim 11 is therefore allowable over the Examiner's cited references.

Claims 18-21

(Reinstated from response filed on 4/22/04) For ease of review, Applicant reproduces independent claim 18 herein below:

18. A cache coherency method comprising:
pausing actions to a cache line;
invalidating said cache line;
modifying said cache line; and
sharing said cache line.

Here the Examiner correctly asserts that the Carpenter reference does not disclose "pausing actions to a cache line" and points to the Parks reference to make up for this outlined deficiency in relation to claim 18 of the present invention. Applicant asserts that there is no suggested desirability in the Carpenter reference to incorporate a step of "pausing actions to a cache line" as recited in claim 18 of the present invention. Accordingly, since there is no suggested desirability in the Carpenter reference to incorporate a step of "pausing actions to a cache line" there is no suggested desirability in the Carpenter reference to be combined with the Parks reference to provide a step of "pausing actions to a cache line" as recited in claim 18 of the present invention. Consequently, claim 18 of the present invention is allowable over the proposed Carpenter-Parks combination of references.

Claims 19-21

Since claims 19-21 are dependent on claim 18, the above-articulated arguments with regard to claim 18 apply with equal force to claims 19-21. Accordingly, claims 19-21 should be allowed over the Examiner's proposed combination of references.

Claims 1-2

For ease of review, Applicant reproduces independent claim 11 herein below:

1. A coherency maintenance system comprising:

a plurality of cache memories including a cache line for storing information;

a plurality of processor cores included on a single substrate for processing instructions and information stored in said plurality of cache memories wherein one of said plurality of processor cores is coupled to and associated with one of said plurality of cache memories; and

a coherency system bus for communicating information between said plurality of cache memories and said plurality of processor cores in accordance with a coherency protocol, wherein said coherency protocol associates a pending state with said cache line.

The Examiner states:

> **Claims 1-2, 12-17, and 18-21 are rejected under 35 U. S. C. 103(a) as being unpatentable over Carpenter et al. (Carpenter) US Patent No. 6,115,804 in view of Parks US Patent No. 6,356,983 and further in view of Cherabuddi US Patent Application Pub No. 2002/0184445.**

Applicant respectfully disagrees. As stated above, when making an obvious rejection under 35 U.S.C. § 103, a necessary condition is that the reference or combination of the cited references ***must teach or suggest all claim limitations.*** (Emphasis added.) If the cited reference(s) do not teach or suggest every element of the claimed invention, then the cited reference(s) fail to render obvious the claimed invention, i.e. the claimed invention is distinguishable over the combination of the cited reference(s).

Additionally, although an Examiner may suggest that the structure of a primary prior art reference *could* be modified in view of a secondary prior art reference to form the claimed structure, the mere fact that the prior art *could* be so modified would not

make the modification obvious unless the prior art suggested the desirability of the modifications. *In re Laskowski.*, 871 F.2d 115, 10 USPQ2d 1297 (CAFC 1989). Motivation cannot be established based on the Applicant's specification. Based on the above-referenced line of reasoning, Applicant asserts that the present invention of claim 1 is not obvious in light of the Examiner's proposed combination.

Firstly, for the reasons outlined above in relation to the rejection of claim 11, Applicant asserts that the Carpenter-Cherrabuddi reference does not teach or suggest every element of the recited invention of claim 1. Specifically, claim 1 recites a plurality of processor cores on a single substrate and the implementation of a coherency system bus. Based on the above-disclosed arguments, Applicant asserts that Carpenter does not teach or suggest these elements of the present invention and it would be improper to combine the Carpenter reference with the Cherrabuddi reference. Since the Carpenter reference does not teach or suggest every element of claim 1 and it would be improper to combine the Carpenter reference with the Cherrabuddi reference, the recited invention of claim 1 is allowable over the Examiner's proposed combination of references.

Claim 2

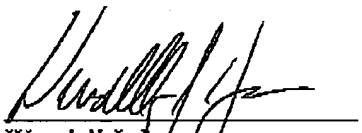
Since claim 2 is dependent on claim 1, the above-articulated arguments with regard to claim 1 apply with equal force to claim 2. Accordingly, claim 2 should be allowed over the Examiner's proposed combination of references.

Claims 12-17

Insofar as neither the Parks reference nor the Cherabuddi reference fails to correct the outlined deficiency of the Carpenter reference, Applicant asserts that the Examiner's proposed combination of references does not teach or suggest the limitations as recited in claim 11 of the present invention. Furthermore, since claims 12-17 are dependent on claim 11, the above-articulated arguments with regard to claim 11 apply with equal force to claims 12-17. Accordingly, claims 12-17 should be allowed over these references.

Applicant believes that this application is in condition for allowance. Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,



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